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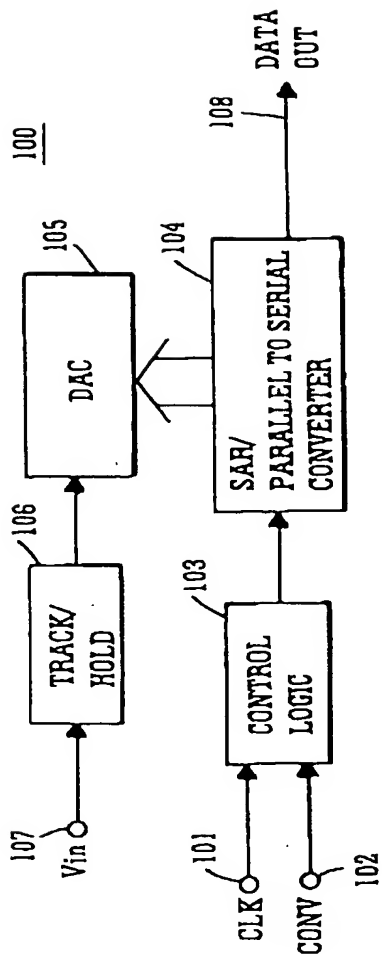
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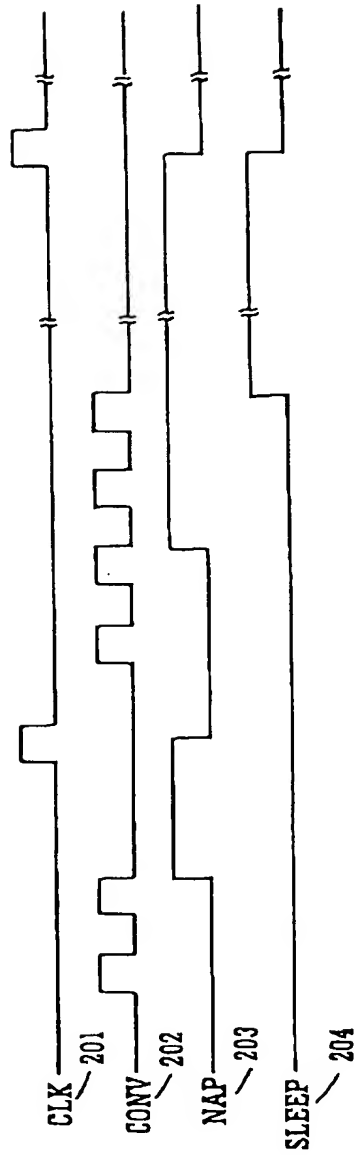
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PRIOR ART  
FIG. 1



PRIOR ART  
FIG. 2

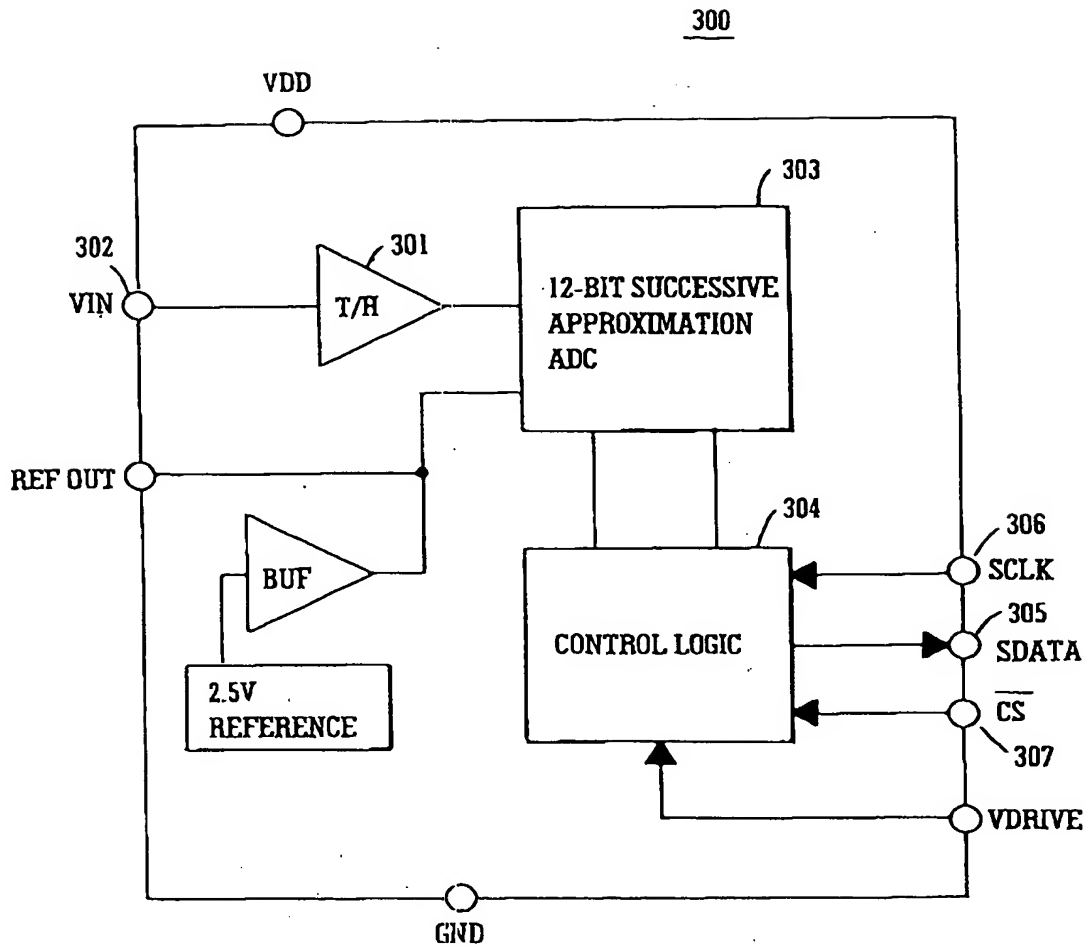


FIG. 3

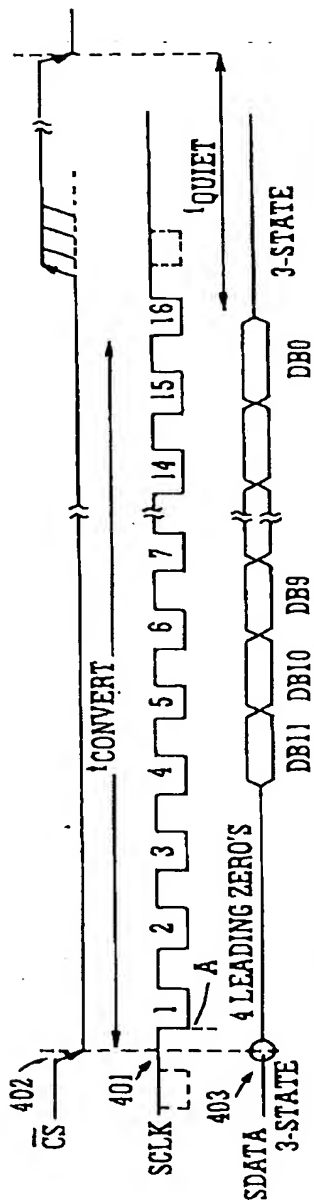


FIG. 4

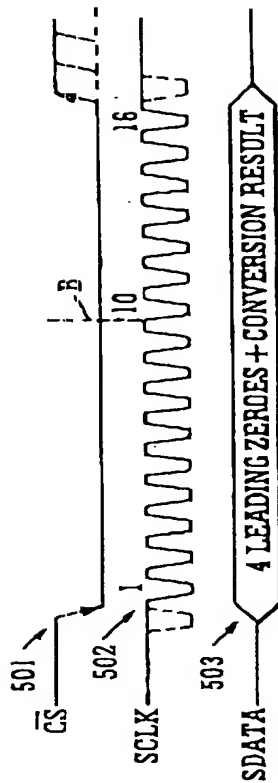


FIG. 5

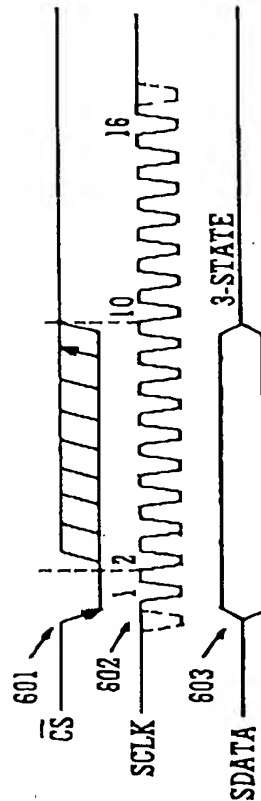
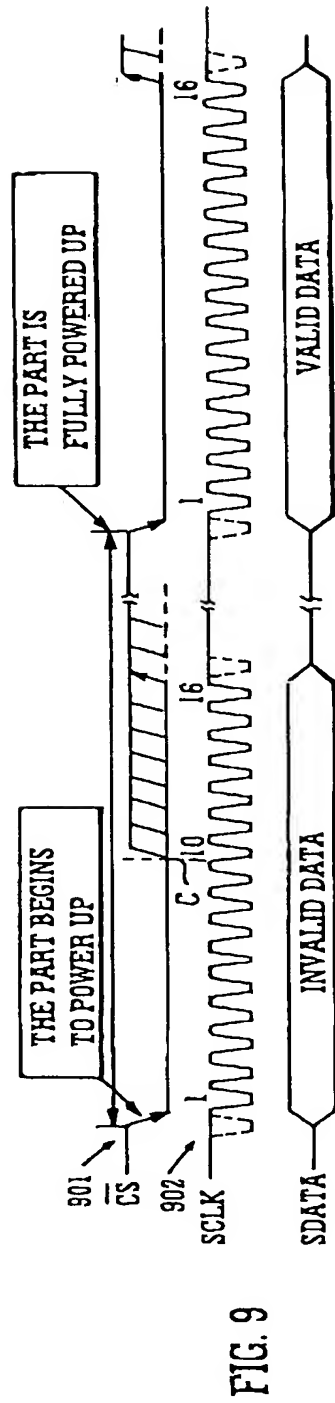
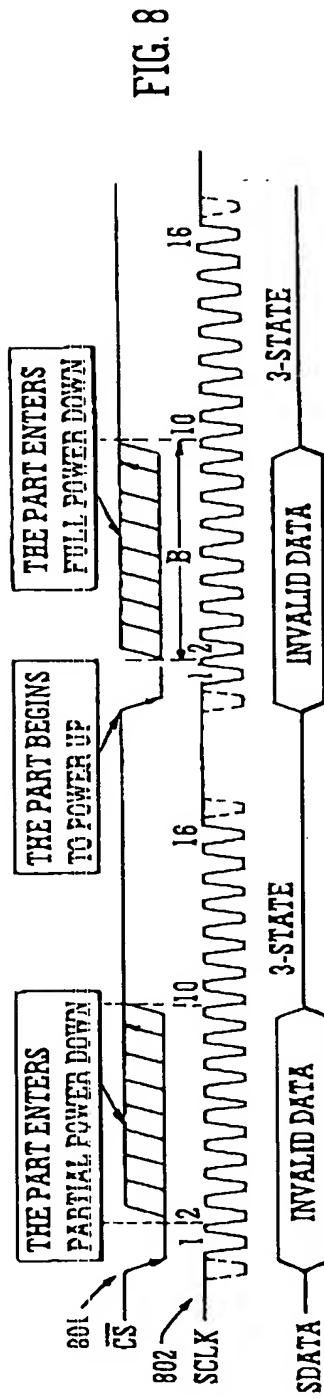
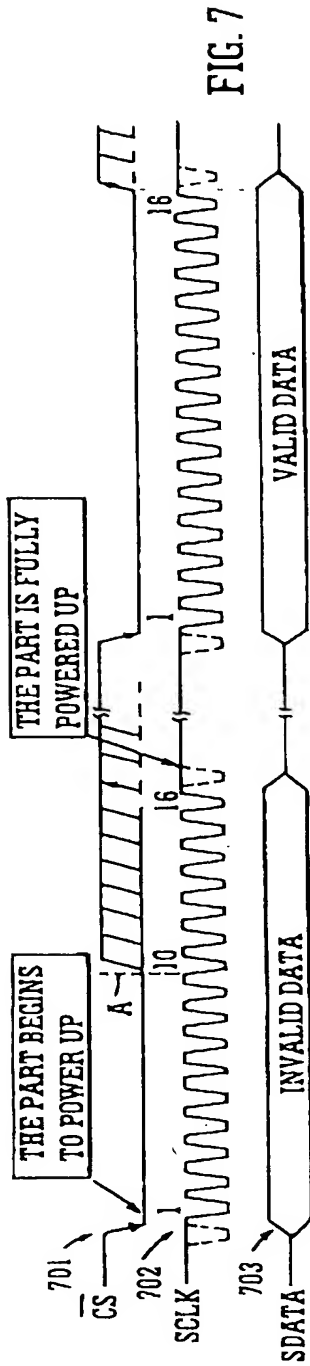
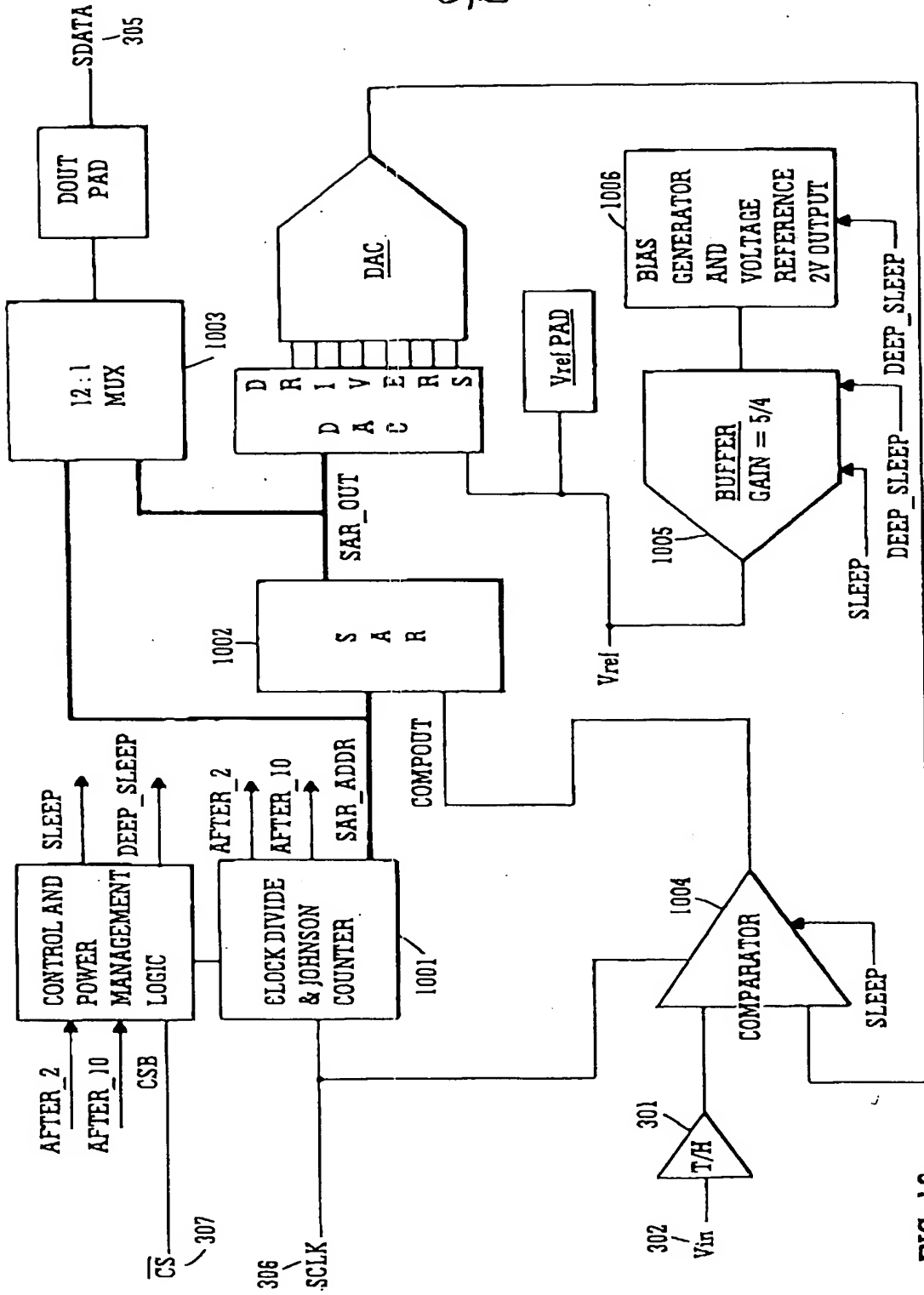


FIG. 6





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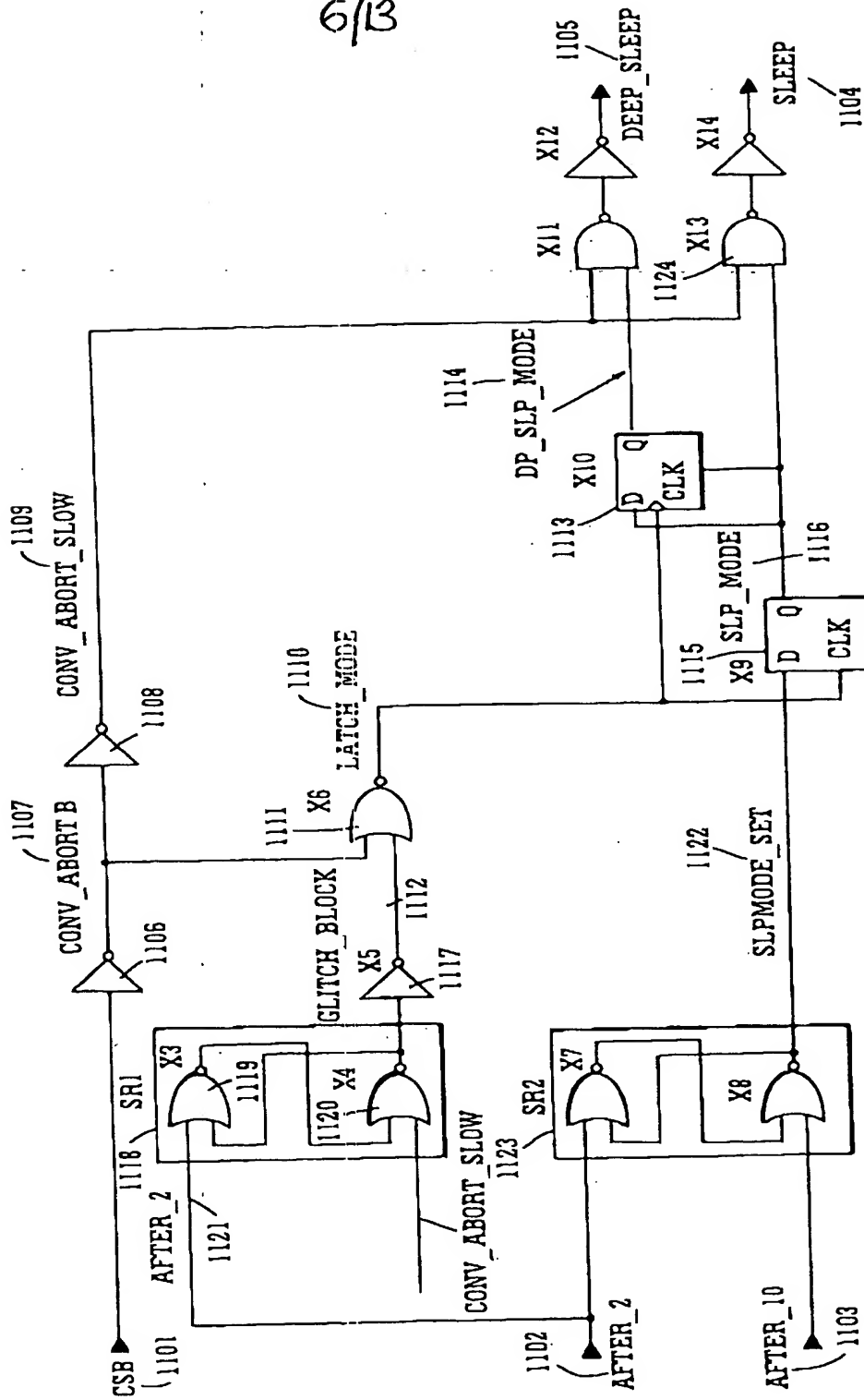


FIG. 11

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1205

1207

1206

1201

307

306

1209

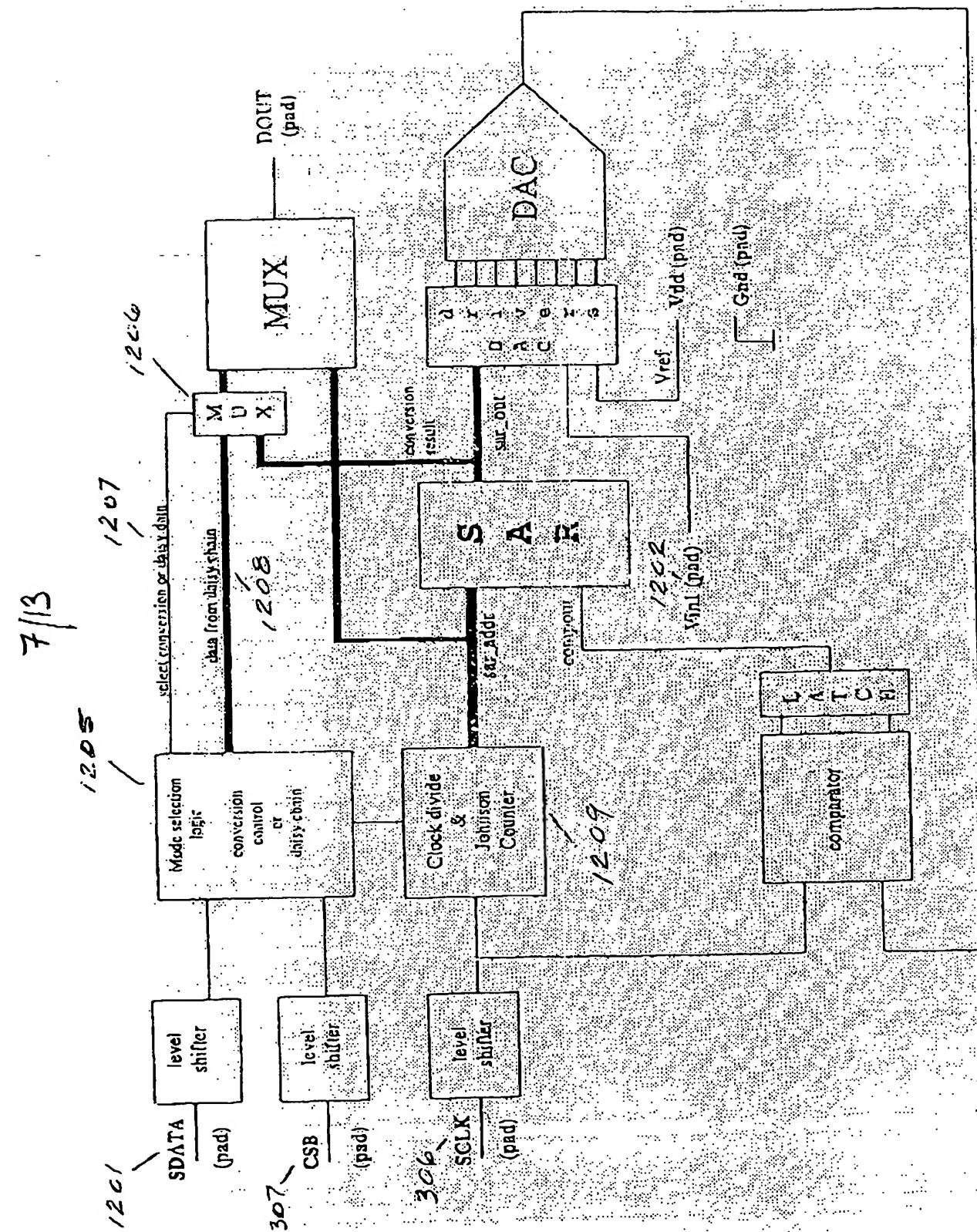


Fig. 12



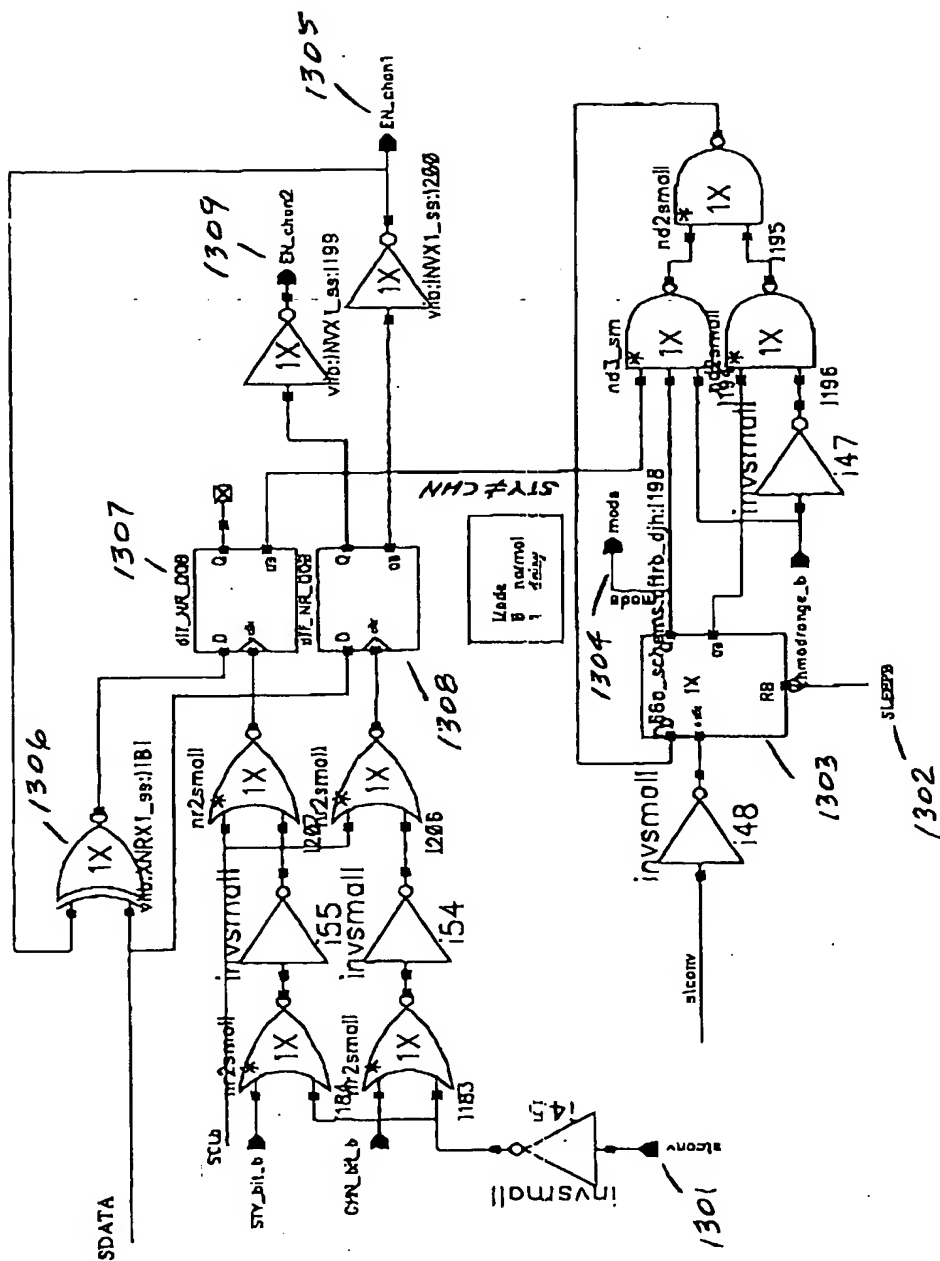
$$\frac{5}{8}$$


Fig. 13

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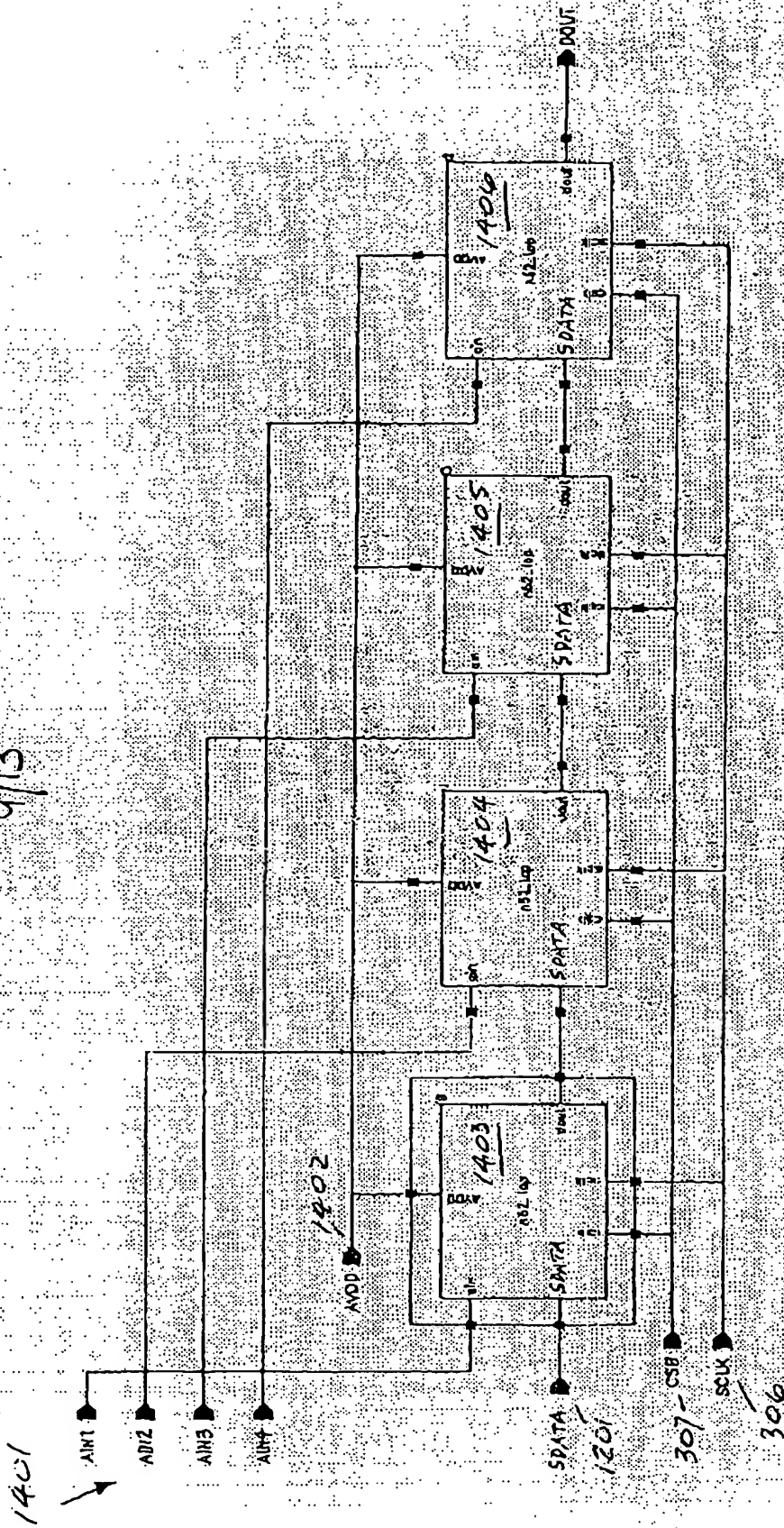


FIG. 14

10/13

Input data word format

0	0	CHN <sub>i</sub>	STY	<data>
---	---	------------------	-----	--------

FIG 15

Output data word format

0	0	CHN <sub>o</sub>	MOD	<data>
---	---	------------------	-----	--------

FIG 16

11/13

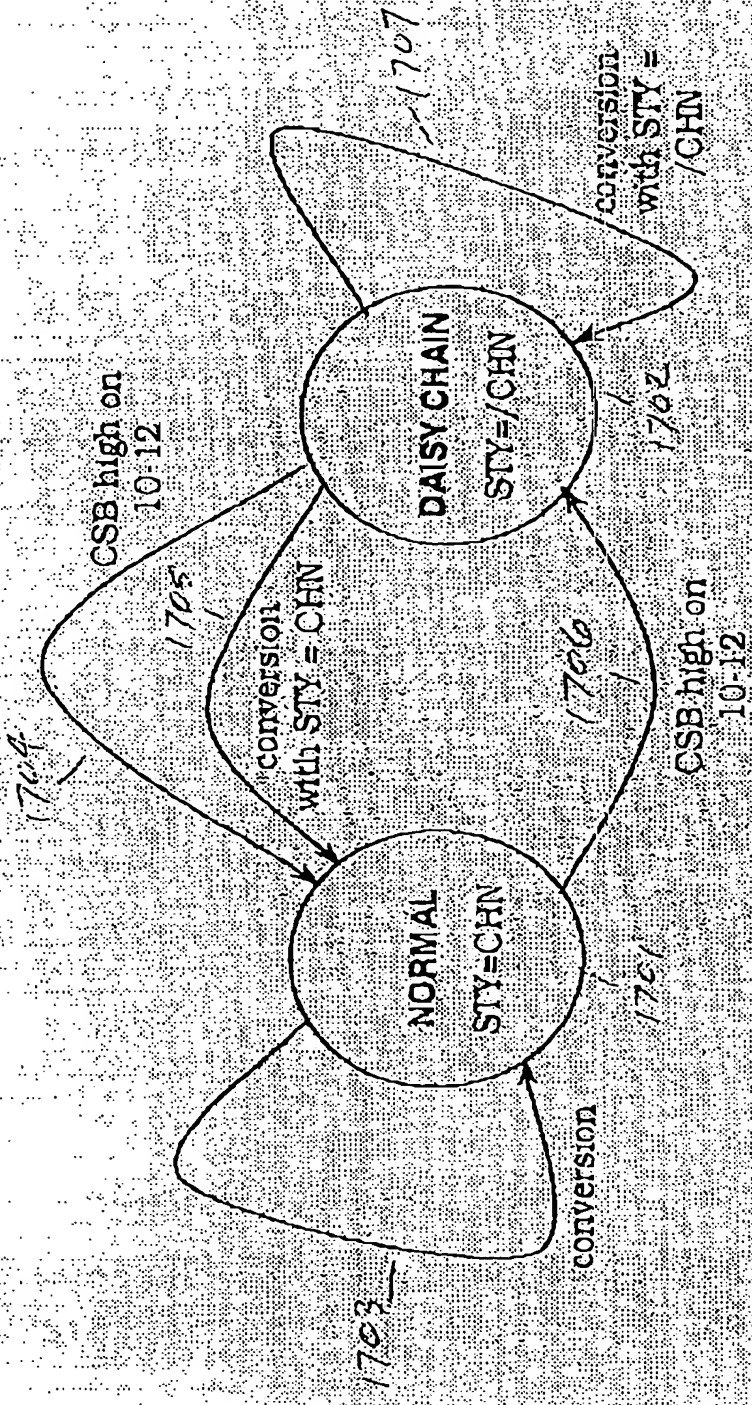
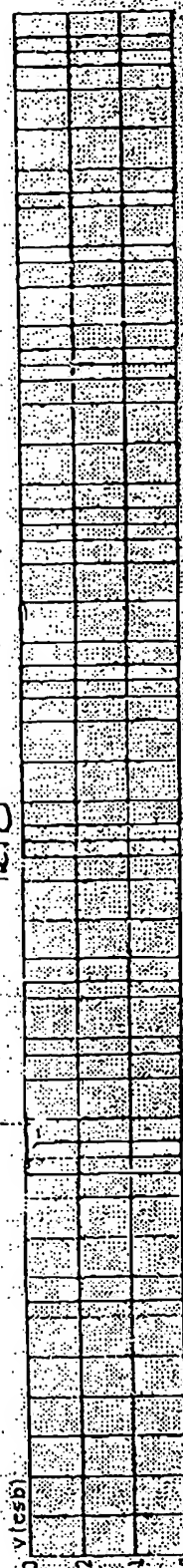


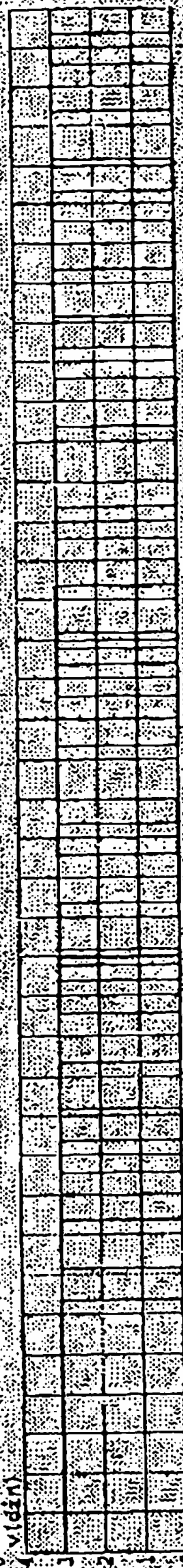
FIG. 17



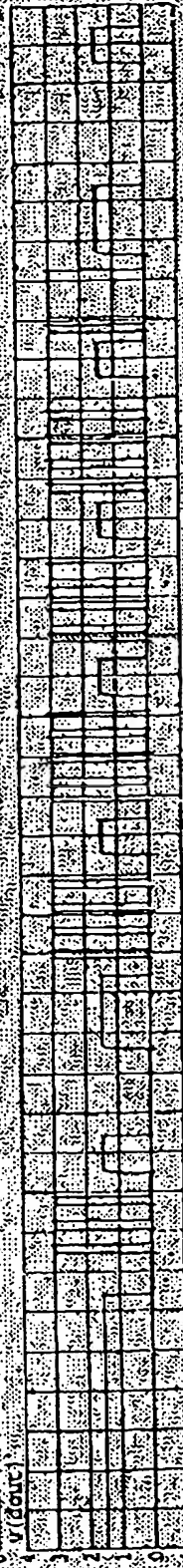
12/13



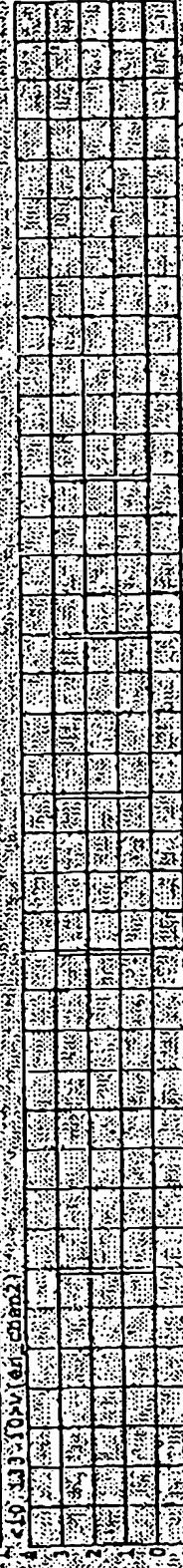
1801 →



1802 →



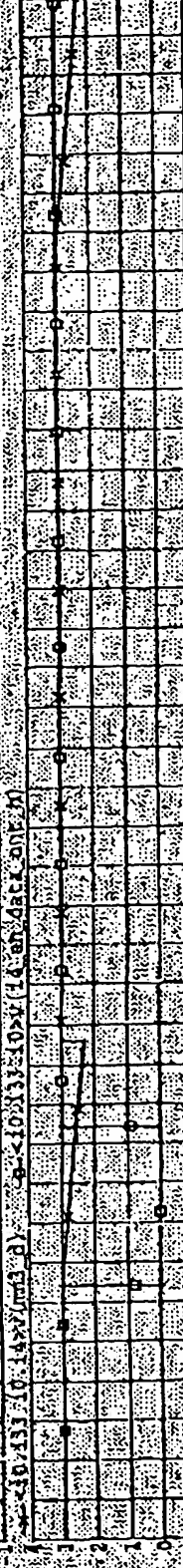
1803 →



1804 →



1805 →



1806 →

TIME  
5.5 6 6.5 7 7.5 8 8.5 9 9.5 10 10.5 11 11.5 12 12.5 13 13.5 14 14.5 15

A B C D E F G H I

F/G:18

13/13

1901

307

level shifter

Mode selection logic  
conversion control and range select

MUX

DOUT (pad)

306

level shifter

Clock divide & Johnson Counter

SAR

DAC

Digital to Analog Converter

conversion result

SAR\_out

SAR\_addr

compar

LATCH

comparator

Vref (pad)

Vin1 (pad)

Vdd (pad)

Gnd (pad)

Fig. 19